Vertical Ge Gate-All-Around Nanowire pMOSFETs with a Diameter down to 20 nm

Mingshan Liu, Stefan Scholz, Alexander Hardtdegen, Jin Hee Bae, Jean-Michel Hartmann, Joachim Knoch, Detlev Grützmacher, Dan Buca, and Qing-Tai Zhao.

***Abstract*—In this work, we demonstrate vertical Ge gate-all-around (GAA) nanowire pMOSFETs fabricated with a CMOS compatible top-down approach. Vertical Ge nanowires with diameters down to 20 nm and an aspect ratio of ~11 were achieved by optimized Cl_2-based dry etching and self-limiting digital etching. Employing a GAA architecture, post-oxidation passivation and NiGe contacts, high performance Ge nanowire pMOSFETs exhibit low SS of 66 mV/dec, small DIBL of 35 mV/V and a high I_{ON}/I_{OFF} ratio of 2.1×10^6. The electrical behavior was also studied with temperature-dependent measurements. The deviation between the experimental SS and the ideal kT/q•ln10 values stems from the density of interface traps (D_{it}). Our measurements suggest that lowering the top contact resistance is a key to further performance improvement of vertical Ge GAA nanowire transistors.**

***Index Terms*—Vertical, Ge, GAA, Nanowire, pMOSFETs**

I. Introduction

To keep up the continuous downscaling of transistors for high performance and low power applications, GAA nanowire transistors have become promising candidates, which can necessitate superior gate electrostatic control over channel and suppress short-channel effects [1]. For ultimately scaled CMOS architecture, the vertical GAA nanowire approach can outperform horizontal GAA nanowire and FinFETs in terms of device layout area, switching speed and power consumption [2-3]. In addition, a vertical nanowire design decouples footprint scaling from gate length scaling, which targets sub-10 nm technology nodes. While bottom-up and top-down approaches have been utilized to fabricate vertical GAA nanowire FETs, the former one is greatly affected by metallic contamination due to the usually adopted Au catalysts. In contrast, the latter approach employs standard CMOS processing techniques to achieve good reproducibility and a precise control of diameter as well as excellent positioning of the nanowires.

Ge is a promising semiconductor for transistors due to its high carrier mobilities and a small bandgap. Thanks to Fermi level pinning close to E_v, Ge p-type planar FETs, FinFETs and horizontal nanowire transistors have been fabricated and achieved high performance [4-20]. However, there is still a lack of investigation on vertical Ge GAA nanowire pFETs.

In this letter, vertical Ge GAA nanowire pMOSFETs fabricated with a top-down approach are reported. An optimized dry etching process to pattern vertical nanowires and digital etching to shrink the nanowire diameters were developed, providing a robust method in forming ultra-scaled nanowires. Sub-20 nm Ge nanowire pMOSFETs with superior performance were obtained. Room temperature characteristics as well as temperature dependence of electrical behaviors were investigated and discussed here.

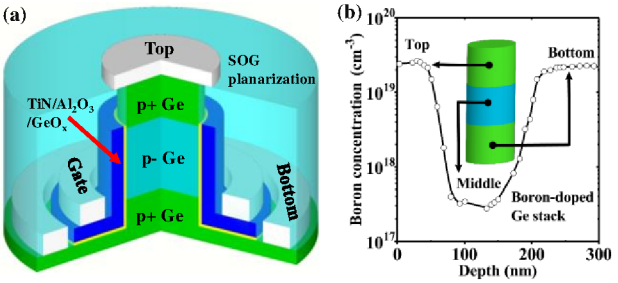

Fig. 1 (a) Three-dimensional schematic of a vertical Ge GAA nanowire pMOSFET with top contact, gate and bottom contact. Spin-on Glass (SOG) was used for the interlayer planarization. (b) Electrochemical C-V (ECV) measurement of active Boron doping concentration in the epi-stacks along the nanowire. The top/bottom Ge layers show ~ 2.5×10^{19} cm^{-3} p-type doping.

II. Vertical Ge Nanowire pFETs Fabrication

Fig. 1(a) presents the 3D cross sectional schematic of a vertical Ge GAA nanowire pMOSFET with top, gate and bottom contacts. The device fabrication started with a Ge strain-relaxed buffer growth by CVD on 200 mm Si (001) wafers. A low temperature (400°C) / high temperature (750°C) approach were used to that end, afterwards with a short duration thermal cycling between 750°C and 875°C to lower the threading dislocations density with 10^7 cm^{-2} values [21]. The Ge:B / Ge / Ge:B stack was grown at 600°C and 100 Torr with GeH_4 and B_2H_6 using [22] data points. The active Boron doping along the vertical direction, measured by Electrochemical Capacitance-Voltage (ECV) method was ~ 2.5×10^{19} cm^{-3} in the top/bottom epi-layers and unintentionally p-type doping with ~ 3×10^{17} cm^{-3} in the middle layer as shown in Fig. 1(b). The designed devices using this material stack work in the accumulation mode. Negative resist Hydrogen SylsesQuioxane (HSQ) was spin-coated and electron beam lithography (EBL) was used to pattern the vertical Ge nanowires. To this end, an optimized Cl_2-based recipe using inductively coupled plasma reactive ion etching (ICP-RIE) was developed to avoid undercutting or micro-trenching effect during the vertical nanowire etching [23]. The nanowire with a 35 nm diameter shown in Fig. 2 (a) has a vertical profile with perfect anisotropy. To further shrink the nanowire size and eliminate RIE-induced damage, digital

This work was supported by the German BMBF project „SiGeSn NanoFETs."

M. Liu, A. Hardtdegen, J. H. Bae, D. Grützmacher D. Buca and Q.-T. Zhao are with Peter-Grünberg-Institute (PGI) and JARA-Fundamentals of Future Information Technologies, Forschungszentrum Jülich, 52428, Germany. (e-mail: m.liu@fz-juelich.de; q.zhao@fz-juelich.de)

S. Scholz, and J. Knoch are with Institute of Semiconductor Electronics, RWTH Aachen University, 52056 Aachen, Germany.

J.-M. Hartmann is with CEA, LETI, MINATEC Campus and University of Grenoble Alpes, 38054 Grenoble, France.

etching comprising multiple cycles of self-limiting O_2 plasma oxidation and diluted HF (1%) stripping was applied. After 10 cycles' digital etching, the diameter of the nanowire was shrunk from 35 nm to 20 nm, as indicated in Fig. 2 (b). An approximate radial etching rate of ~0.75 nm per cycle was extracted. It is also shown that cyclic digital etching for as-grown Ge samples contributes to a reduced root mean square (RMS) surface roughness as confirmed with Atomic Force Microscope (AFM) measurements [23-24].

Subsequently, a multi-step high-κ dielectric deposition was used to improve the high-κ/Ge interface for a low D_{it}. 1 nm Al_2O_3 was first deposited in the ALD chamber, followed by a post-oxidation process at 500 ºC for 1min. Then, 8 nm Al_2O_3 deposition and 40 nm TiN sputtering were conducted. They wrapped around the vertical nanowire, forming the gate stack (Fig. 2 (c)). Note that the sputtering in this work leads to conformal coverage with a sidewall thickness roughly half of that on the planar surface. Fig. 2 (d) displays a high-resolution TEM (HR-TEM) image of the high-κ/metal gate stack on the nanowire sidewall, showing excellent quality of the gate stack and good crystallinity of Ge channel. The GeO_x interfacial layer (IL) generated underneath Al_2O_3 layer is clearly visible with the thickness of ~2 nm.

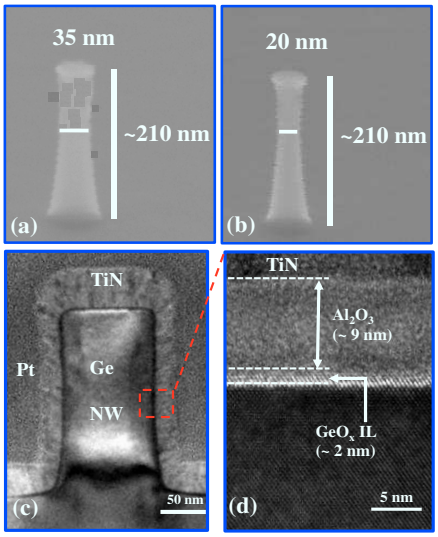

Fig. 2 (a) Vertical Ge nanowire with a 35 nm diameter exhibiting a perfect anisotropy (b) The nanowire in (a) was scaled to a 20 nm diameter and an aspect ratio of 10.5 after 10 cycles' digital etching. (c) Cross-sectional TEM image of a vertical Ge nanowire with a TiN/Al_2O_3/GeO_x gate stack. (d) HR-TEM image of gate stack, depicting excellent quality of the gate stack and good crystallinity of Ge channel.

After gate patterning, a forming gas annealing (FGA) at 400 ºC was performed to annihilate traps inside the dielectric. To define the vertical transistor physical TiN gate length, SOG resist was spin-coated and cured at 350 ºC in a N_2 environment, serving as a planarization layer. The removal of the top gate stack was then carried out by an optimized isotropic dry etching recipe, leaving the top nanowire region exposed for the top contact. Thus, the physical gate length is determined by the planarization thickness of SOG, which to a large degree, relaxes the lithographic limits facing the current semiconductor industry. Afterwards, a second SOG planarization was performed as the spacer insulation of the gate. 6 nm Ni was sputtered to form the NiGe top contact using lift-off and FGA techniques. Next, via window opening by CHF_3 plasma was used to expose the buried gate and the bottom region. Finally, the device fabrication ended with Ti/Al contact pads and post metallization annealing (PMA).

III. Results and Discussion

Throughout this work, the transistors are measured with top contact as drain configuration and the normalization is conducted by the nanowire perimeter (π × diameter).Fig. 3(a) depicts the I_D-V_{GS} transfer characteristics of a single vertical Ge GAA nanowire pMOSFET with a 20 nm diameter. The gate length is 150 nm. Thanks to the excellent gate electrostatic integrity provided by the 3D GAA nanowire architecture, the post-oxidation passivation method and NiGe contacts, the device achieves superior performance with low SS of 66 mV/dec, small DIBL of 35 mV/V and an I_{ON}/I_{OFF} ratio of 2.1×10^6 at V_{DS} = -0.1V. Note that SS is extracted as the average slope over two orders of magnitude of I_D. The peak extrinsic transconductance $G_{max,ext}$ is ~95 μS/μm at V_{DS} = -0.5V. I_D-V_{DS} output curves of the corresponding Ge pFET at V_{GS} ranging from 0V to -1V are plotted in Fig. 3(b), showing good current saturation. The I_D achieves 52 μA/μm at V_{GS}= V_{DS} = -1V.

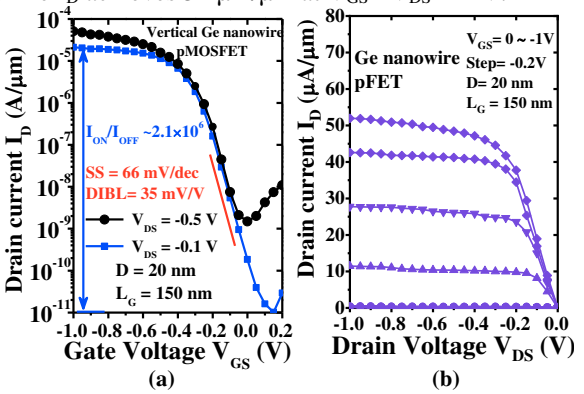

Fig. 3. (a) I_D-V_{GS} transfer characteristics of a single vertical Ge GAA nanowire pMOSFET with a 20 nm diameter: low SS of 66 mV/dec, small DIBL of 35 mV/V and an I_{ON}/I_{OFF} ratio of 2.1×10^6 at V_{DS} = -0.1V. (b) I_D-V_{DS} output curves of the corresponding Ge pFET at V_{GS} from 0 to -1V, showing good current saturation.

The total resistance R_{tot} for the 20 nm diameter Ge nanowire pMOSFET is calculated to be 16 kΩ·μm at V_{GS} -V_{TH} = V_{DS} = -0.5V (V_{TH} is determined at 100 nA/μm). This is larger than the extrinsic resistance target (300 Ω·μm) required by the International Roadmap for Devices and Systems (IRDS-2017). In the vertical nanowire architecture, there is an inherent asymmetry between top and bottom resistance. Indeed, the top contact covers only a small nanowire tip while the bottom contact area is relatively larger. Therefore, R_{tot} is dominated by the top contact resistance. This leads to a challenging bottleneck to scale nanowire diameters to a small dimension, which is an issue for all of group III-V and IV vertical nanowire transistors. [25-27].

Novel processing strategies are required to further improve the device performance: (i). Increasing the doping of the top/bottom epi-stacks would result in a small contact resistance, a small R_{tot} and therefore an enhanced I_{ON}. Non-equilibrium methods to promote dopant activation in Ge, e.g. flash lamp annealing or laser annealing are preferred [28-30]; (ii). Scaling the equivalent oxide thickness (EOT) is reasonable to improve SS, I_{ON} etc. (EOT in this work is ~ 5 nm); (iii). Epitaxial growth on top of the nanowire or a gate-last process aimed at increasing the top

contact area may be one option to reduce the top contact resistance [31-32]; (iv). Arrays of nanowire transistors are also a performance booster for reduced parasitic capacitances and improved current drivability [26, 32].

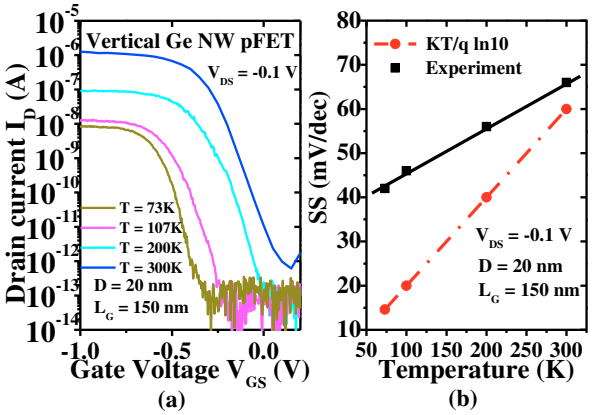

Fig. 4. (a) I_D-V_{GS} curves of a 20 nm nanowire pMOSFET measured at various temperatures ranging from 300K down to 73K and V_{DS}= -0.1V. (b) SS characteristics as a function of temperatures. The difference between ideal and experimental SS lies in D_{it} at the high-κ/nanowire interface.

We also investigate the temperature dependence of the electrical behavior of Ge nanowire pMOSFETs. Fig. 4(a) shows the I_D-V_{GS} curves of a 20 nm nanowire pFET measured at various temperatures ranging from 300K down to 73K. V_{TH} defined at 100 nA/μm shows a decreasing trend with the temperature, which is similar to that of horizontal Si nanowire devices [33]. The on-currents I_{ON} are apparently sensitive to various temperatures. As temperature decreases, I_D becomes unexpectedly smaller, although the mobility enhancement induced by reduction of the phonon scattering should have resulted in higher G_m and I_D. We also found that $G_{m,ext}$ exhibits a decreasing trend with temperatures. We attribute such phenomena to the deteriorated top contact resistance at low temperatures. The increased R_{tot} primarily results from the top contact resistance and yields reduced $G_{m,ext}$ and I_{ON}. This again confirms the significance of a low top contact resistance for vertical nanowire devices. Nevertheless, the SS characteristics in Fig. 4(b) clearly depict the SS reduction with temperatures. The deviation between the experimental SS and the ideal kT/q·ln10 values stems from D_{it} particularly because of the high surface-to-volume ratio in nanowire itself. Hence, the surface passivation should be optimized to improve the interface quality, especially for the ultra-scaled nanowires.

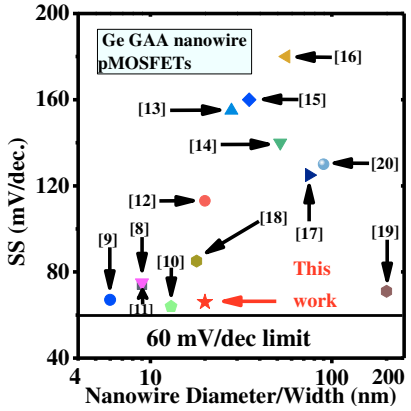

Fig. 5. Benchmark of SS with various nanowire diameters/widths among Ge vertical or lateral GAA nanowire pMOSFETs. This work demonstrates the low SS of 66 mV/decade for vertical Ge nanowire pFETs.

Fig. 5 benchmarks SS with various nanowire diameters or widths among the reported Ge GAA nanowire pMOSFETs in the literature. This work successfully demonstrates high performance vertical GAA nanowire pMOSFETs by the top-down approach. Our device achieves low SS of 66 mV/decade, which is comparable to those SS values in the state-of-the-art horizontal 6 nm and 13 nm diameter nanowire Ge pMOSFETs [9-10].

IV. CONCLUSION

We have presented a fully CMOS compatible top-down method for ultra-scaled vertical Ge GAA nanowire pMOSFETs. Ge pFETs with a sub-20 nm diameter show excellent SS of 66 mV/dec, small DIBL of 35 mV/V and a high I_{ON}/I_{OFF} ratio of 2.1×10^6. Electrical measurements conducted at various temperatures demonstrate the significance of reducing the top contact resistance, which is a challenge specifically for vertical GAA nanowire transistors. The vertical nanowire architecture proposed in this work could potentially enable sub-10 nm technology nodes for the CMOS roadmap.

REFERENCES

[1] R. Ritzenthaler, H. Mertens, V. Pena, G. Santoro, A. Chasin, K. Kenis, K. Devriendt, G. Mannaert, H. Dekkers, A. Dangol, Y. Lin, S. Sun, Z. Chen, M. Kim, J. Mahillot, J. Mitard, N. Yoshida, N. Kim, D. Mocuta, N. Horiguchi, "Vertically stacked gate-all-around Si nanowire CMOS transistors with reduced vertical nanowires separation, new work function metal gate solutions and DC/AC performance optimization," in *IEDM Tech. Dig*., Dec. 2018, pp. 508-511. DOI: 10.1109/IEDM.2018.8614528

[2] A. V. Thean, D. Yakimets, T. H. Bao, P. Schuddinck, S. Sakhare, M. G. Bardon, A. S.-Hernandez, I. Ciofi, G. Eneman, A. Veloso, J. Ryckaert, P. Raghavan, A. Mercha, A. Mocuta, Z. Tokei, D. Verkest, P. Wambacq, K. De Meyer, N. Collaert, "Vertical device architecture for 5 nm and beyond: device & circuit implications," in *Symp. VLSI Technol*., 2015, T26-27. DOI: 10.1109/VLSIT.2015.7223689

[3] D. Yakimets, G. Eneman, P. Schuddinck, T.H. Bao, M.G. Bardon, P. Raghavan, A. Veloso, N. Collaert, A. Mercha, D. Verkest, A.V. Thean, and K. D. Meyer, "Vertical GAAFETs for the ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1433-1439, May 2015. DOI: 10.1109/TED.2015.2414924

[4] J. Mitard, B. De Jaeger, F.E. Leys, G. Hellings, K. Martens, G. Eneman, D.P. Brunco, R. Loo, J.C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C.H. Yu, K.De Meyer, M. Caymax, L. Pantisano, M. Meuris, M. M. Heyns, "Record I_{ON}/I_{OFF} performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability," in *IEDM Tech. Dig*., Dec. 2008, pp. 873-875. DOI: 10.1109/IEDM.2008.4796837

[5] R. Zhang, J. Li, F. Chen, and Y. Zhao, "High performance Germanium pMOSFETs with NiGe metal source/drain fabricated by microwave annealing," *IEEE Trans. Electron Devices*, vol. 63, no. 7, pp. 2665-2670, Jul. 2016. DOI: 10.1109/TED.2016.2564996

[6] T. I. Lee, M.-C. Nguyen, H. J. Ahn, M. J. Kim, E. J. Shin, W. S. Hwang, H.-Y. Yu, R. Choi, and B.J. Cho, "H_2 high pressure annealed Y-doped ZrO_2 gate dielectric with an EOT of 0.57 nm for Ge MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1350-1353, Sep. 2019. DOI: 10.1109/LED.2019.2928026

[7] H. Arimura, L. Witters, D. Cott, H. Dekkers, R. Loo, J. Mitard, L.-A. Ragnarsson, K. Wostyn, G. Boccardi, E. Chiu, A. Subirats, P. Favia, E. Vancoille, V.De Heyn, D. Mocuta, and N. Collaert, "Performance and electrostatic improvement by high-pressure anneal on Si-passivated strained Ge pFinFET and gate all around devices with superior NBTI reliability," in *Symp. VLSI Technol*., 2017, T196-T197. DOI: 10.23919/VLSIT.2017.7998169

[8] E. Capogreco, H. Arimura, L. Witters, A. Vohra, C. Pottet, R. Loo, A. De Keersgieter, E. Dupuy, D. Marinov, A. Hikavyy, F. Sebaai, G. Mannaert, L.-A. Ragnarsson, Y.K. Siew, C. Vrancken, A. Opdebeeck, J. Mitard, R. Langer, E. Altamirano, F. Holsteyns, S.

Demuynck, K. Barla, V. De Heyn, D. Mocuta, N. Collaert, N. Horiguchi, "High performance strained Germanium gate all around p-channel devices with excellent electrostatic control for sub-30 nm L_G," in *Symp. VLSI Technol*., 2019, T94-T95. DOI: 10.23919/VLSIT.2019.8776558

[9] M.J.H. van Dal, G. Vellianitis, G. Doornbos, B. Duriez, M.C. Holland, T. Vasen, A. Afzalian, E. Chen, S.K. Su, T.K. Chen, T.M. Shen, Z.Q. Wu, C.H. Diaz, "Ge CMOS gate stack and contact development for vertically stacked lateral nanowire FETs," in *IEDM Tech. Dig.*, Dec. 2018, pp. 492-495. DOI: 10.1109/IEDM.2018.8614577

[10] E. Capogreco, L. Witters, H. Arimura, F. Sebaai, C. Pottet, A. Hikavyy, R. Loo, A. P. Milenin, G. Eneman, P. Favia, H. Bender, K. Wostyn, E. Dentoni Litta, A. Schulze, C. Vrancken, A. Opdebeeck, J. Mitard, R. Lander, F. Holsteyns, N. Waldron, K. barla, V.De Heyn, D. Mocuta, N. Collaert, "First demonstration of vertically-stacked gate-all-around highly-strained Germanium nanowire p-FETs," in *Symp. VLSI Technol*., 2018, 193-194. DOI: 10.1109/VLSIT.2018.8510645

[11] L. Witters, F. Sebaai, A. Hikavyy, A. P. Milenin, R. Loo, A. De keersgieter, G. Eneman, T. Schram, K. Wostyn, K. Devriendt, A. Schulze, R. Lieten, S. Bilodeau, E. Cooper, P. Storck, C. Brancken, H. Arimura, P. Favia, E. Vancoille, J. Mitard, R. Langer, A. Opdebeeck, F. Holsteyns, N. Waldron, K. Barla, V. De Heyn, D. Mocuta, N. Collaert, "Strained Germanium gate-all-around PMOS device demonstration using selective wire release etch prior to replacement metal gate deposition," in *Symp. VLSI Technol*., 2017, T194-T195. DOI: 10.23919/VLSIT.2017.7998168

[12] H. Wu, W. Wu, M. Si, and P. D. Ye, "First demonstration of Ge nanowire CMOS circuits: lowest SS of 64 mV/dec, highest g_{max} of 1057 μS/μm in Ge nFETs and highest maximum voltage gain of 54V/V in Ge CMOS inverters," in *IEDM Tech. Dig.*, Dec. 2015, pp. 15-19. DOI: 10.1109/IEDM.2015.7409610

[13] K. Ikeda, Y. Kamimuta, Y. Moritama, M. Ono, K. Usuda, M. Oda, T. Irisawa, K. Furuse and T. Tezuka, "Enhancement of hole mobility and cut-off characteristics of strained Ge nanowire pMOSFETs by using plasma oxidized GeO_x inter-layer for gate stack," in *Symp. VLSI Technol*., 2013, T30-T31.

[14] S.-H. Hsu, C.-L. Chu, W.H. Tu, Y.-C. Fu, P.-J. Sung, H.-C. Chang, Y.-T. Chen, L.Y. Cho, W. Hsu, G.-L. Luo, C.W. Liu, C. Hu and F.L. Yang, "Nearly defect-free Ge gate-all-around FETs on Si substrates," in *IEDM Tech. Dig.*, Dec. 2011, pp. 825-828. DOI: 10.1109/IEDM.2011.6131676

[15] J.W. Peng, N. Singh, G.Q. Lo, D.L. Kwong and S.J. Lee, "CMOS compatible Ge/Si core/shell nanowire gate-all-around pMOSFET integrated with HfO_2/TaN gate stack," in *IEDM Tech. Dig.*, Dec. 2009, pp. 931-934. DOI: 10.1109/IEDM.2009.5424284

[16] J. Nah, E.-S. Liu, K. M. Varahramyan, D. Shahrjerdi, S. K. Banerjee, and E. Tutuc, "Scaling properties of Ge-Si_xGe_{1-x} core-shell nanowire field effect transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 491-495, 2010. DOI: 10.1109/TED.2009.2037406

[17] R. Cheng, B. Liu, R. Guo ,Y. Yang, Q. Zhou, X. Gong, Y. Tong, K. Bourdelle, N. Daval, D. Delprat, B.-Y. Nguyen, E. Augendre, Y.-C.Yeo "Asymmetrically strained high performance Germanium gate-all-around nanowire p-FETs featuring 3.5nm wire width and contractible phase change liner stressor($Ge_2Sb_2Te_5$)," in *IEDM Tech. Dig.*, Dec. 2013, pp. 653-656. DOI: 10.1109/IEDM.2013.6724699

[18] W. Chern, P. Hashemi, J. T. Teherani, T. Yu, Y. Dong, G. Xia, D.A. Antoniadis and J. L. Hoyt, "High mobility high-κ-all-around asymmetrically-strained Germanium nanowire trigate p-MOSFETs," in *IEDM Tech. Dig.*, Dec. 2012, pp. 387-390. DOI: 10.1109/IEDM.2012.6479055

[19] J. Feng, G. Thareja, M. Kobayashi, S. Chen, A. Poon, Y. Bai, P. B. Griffiin, S. S. Wong, T. Nishi, and J.D. Plummer, "High performance gate-all-around GeOI p-MOSFETs fabricated by rapid melt growth using plasma nitridation and ALD Al_2O_3 gate dielectric and self-aligned NiGe contacts," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 805-807, July 2008. DOI" 10.1109/LED.2008.2000613

[20] C.-L. Chu, K. Wu, G.-L. Luo, B.-Y. Chen, S.-H. Chen, W.-F. Wu, and W.-K. Yeh, "Stacked Ge-nanosheet GAAFETs fabricated by Ge/Si multilayer epitaxy," *IEEE Electron Device Lett.,* vol. 39, no. 8, pp. 1133-1136, August 2018. DOI: 10.1109/LED.2018.2850366

[21] J.M. Hartmann and J. Aubin, "Assessment of the growth/etch back technique for the production of Ge strain-relaxed buffers on Si," *Journal of Crystal Growth*, vol. 488, pp. 43–50, 2018. DOI: 10.1016/j.jcrysgro.2018.02.036

[22] Y. Bogumilowicz and J.M. Hartmann, "Reduced-pressure chemical vapor deposition of boron-doped Si and Ge layers," *Thin Solid Films*, vol. 557, pp. 4-9, 2014. DOI: 10.1016/j.tsf.2013.08.037

[23] M. Liu, K. Mertens, S. Glass, S. Trellenkamp, S. Mantl, D. Buca, and Q.-T. Zhao. "Realization of vertical Ge nanowires for gate-all-around transistors," In *EUROSOI-ULIS*, April 2018, pp.1-4. DOI: 10.1109/ULIS.2018.8354771

[24] W. Wang, L.Dian, Y. Dong, X. Gong, E. S. Tok, and Y. C. Yeo, "Digital etch technique for forming ultra-scaled Germanium-Tin ($Ge_{1-x}Sn_x$) Fin structure," *Scientific Reports*, vol. 7, no. 1, pp. 1-9, May, 2017. DOI: 10.1038/s41598-017-01449-1

[25] X. Zhao, C. Heidelberger, E.A. Fitzgerald, W. Lu, A. Vardi, and J.A. Del Alamo, "Sub-10 nm diameter InGaAs vertical nanowire MOSFETs," in *IEDM Tech. Dig.*, Dec. 2017, pp. 413-416. DOI: 10.1109/IEDM.2017.8268407

[26] Y. Guerfi and G. Larrieu, "Vertical Silicon nanowire field effect transistors with nanoscale gate-all-around," *Nanoscale Research Lett.*, vol. 11, no. 1, pp. 210-216, 2016. DOI: 10.1186/s11671-016-1396-7

[27] A. Veloso, B. Parvais, P. Matagne, E. Simoen, T. Huynh-Bao, V. Paraschiv, E. Vecchio, K. Devriendt, E. Rosseel, M. Ercken, B.T. Chan, C. Delvaux, E. Altamirano-Sanchez, J.J. Versluijs, Z. Tao, S. Suhard, S. Brus, A. Sibaja-Hernandez, N. Waldron, P. Lagrain, O. Richard, H. Bender, A. Chasin, B. Kaczer, T. Ivanov, S. Ramesh, K.De Meyer, J. Ryckaert. N. Collaert and A. Thean, "Junctionless gate-all-around lateral and vertical nanowire FETs with simplified processing for advanced logic and analog/RF applications and scaled SRAM cells," in *Symp. VLSI Technol*., 2016, 138-139. DOI: 10.1109/VLSIT.2016.7573409

[28] S. Prucnal, J. Frigerio, E. Napolitani, A. Ballabio, Y. Berencen, L. Rebohle, M. Wang, R. Bottger, M. Voelskow, G. Isella, R. Hubner, M. Helm, S. Zhou, and W. Skorupa, "In situ ohmic contact formation for n-type Ge via non-equilibrium processing," *Semicond. Sci. Technol.*, vol. 32, no. 11, pp. 115006:1-7. DOI: 10.1088/1361-6641/aa8b2f

[29] S.-H. Huang, F.-L. Lu, W.-L. Huang, C.-H. Huang, and C.W. Liu, "The ~3×10^{20} cm^{-3} electron concentration and low specific contact resistivity of phosphorus doped Ge on Si by in-situ chemical vapor deposition doping and laser annealing," *IEEE Electron Device Lett.*, vol. 36, no. 11, pp. 1114-1117, July 2015. DOI: 10.1109/LED.2015.2478916

[30] O. Gluschenkov, H. Wu, K. Brew, C. Niu, L. Yu, T. Sulehria, S. Choi, C. Durfee, J. Demarest, A. Carr, S. Chen, J. Willis, T. Thanigaivelan, F.-L. Lie, W. Kleemerier and D. Guo, "External resistance reduction by nanosecond laser anneal in Si/SiGe CMOS technology," in *IEDM Tech. Dig.*, Dec. 2018, pp. 815-818. DOI: 10.1109/IEDM.2018.8614628

[31] M. Berg, K.-M. Persson, O.-P. Kilpi, J. Svensson, E. Lind and L.-E. Wernersson, "Self-aligned, gate-last process for vertical InAs nanowire MOSFETs on Si," in *IEDM Tech. Dig.*, Dec. 2015, pp. 803-806. DOI: 10.1109/IEDM.2015.7409806

[32] O.-P. Kilpi, J. Svensson, and L.-E. Wernersson, "Sub-100 nm gate-length scaling of vertical InAs/InGaAs nanowire MOSFETs on Si," in *IEDM Tech. Dig.*, Dec. 2017, pp. 417-420. DOI: 10.1109/IEDM.2017.8268408

[33] N. Singh, F.Y. Lim, W.W. Fang, S.C. Rustagi, L.K. Bera, A. Agarwal, C.H. Tung, K.M. Hoe, S.R. Omampuliyur, D. Tripathi, A.O. Adeyeye, G.Q. Lo, N. Balasubramanian, and D.L. Kwong, "Ultra-narrow Silicon nanowire gate-all-around CMOS devices: Impact of diameter, channel-orientation and low temperature on device performance," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1-4. DOI: 10.1109/IEDM.2006.346840